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Research on Power Factor Correction Boost Inductor Design

Optimization – Efficiency vs. Power Density

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Abstract-- Nowadays, efficiency and power density are the most important issues for Power Factor Correction (PFC) converters development. However, it is a challenge to reach both high efficiency and power density in a system at the same time. In this paper, taking a Bridgeless PFC (BPFC) as an example, a useful compromise between efficiency and power density of the Boost inductors on 3.2kW is achieved using an optimized design procedure. The experimental verifications based on the optimized inductor are carried out from 300W to 3.2kW at 220Vac input.

Index Terms-- Boost Inductor; Optimization; Bridgeless PFC; Efficiency; Power Density

I. INTRODUCTION

With the increasing demands on Green Power Electronics in the global-world, more and more countries have been requiring the power supplies to meet certain standards in order to reduce their Electronics Pollutions to the Grid. Therefore, Power Factor Correction (PFC) converters have been picked up momentum, and novel Bridgeless PFC (BPFC) topologies have been invented to improve the performances and power density [1]–[5]. However, because of the native advantages - such as - easy circuit and system design, low cost, nice reduction of line harmonics currents, the Boost cell BPFCs still receive most attentions among all the BPFC topologies which came out during recent years.

Boost Inductors play a critical role in Boost type PFC converters. On one hand, it affects system efficiency through increasing or reducing semiconductor and magnetic losses depending on its value. On the other hand, assuming a fixed energy store, in the optimized design, the maximum flux density and the winding factor of the core are both on the boundary of limitations; therefore the volume of the inductor, which dominates power density of a PFC, will be determined by the inductance. Facing the biggest challenge in PFC design today – high efficiency vs. high power density, it is necessary to investigate the PFC inductor's operating characteristics and find out how it affects system's efficiency and power density. However, this has been difficult all the time, due to the lack of an effective way for designers to evaluate the overall performances of PFC inductors.

In order to optimize the inductor design in PFC converters, the questions below should be taken into consideration:

1. Is there any reasonable region to limit the Boost inductance for a certain PFC topology?

2. How to select windings and cores to minimize the magnetic losses while maintain high power density?

By answering these questions, in this paper, a useful balance between efficiency and power density of Boost inductor in a Two-Boost-Circuit BPFC is achieved using an optimized design procedure. Generally, based on this procedure, designers will be able to make a reasonable inductor design for any Boost type PFC topologies.

Section II is a brief introduction of high efficiency BPFC topologies. The design procedure is firstly illustrated and showed in a flowchart in section III. In section IV, functions between inductance and semiconductor losses are given with mathematical demonstration. Section V shows the method of getting a compromise of volume and efficiency of a Boost inductor. The relationship of inductance, inductor's volume and power losses is exhibited to clarify the method. In order to demonstrate and validate the procedure, the optimized Boost inductors were tested in the CCM Two-Boost-Circuit BPFC with an output power range from 300W to 3.2kW in section VI. Measured data of system efficiency are compared with those from the calculation based on the optimized design procedure. Section VII comes up with the conclusion.

II. HIGH EFFICIENCY BRIDGELESS PFC TOPOLOGIES

The idea of BPFC goes back to eighties [6]. Reference [7] shows the basic performances of some BPFC topologies. These topologies can be expected having higher efficiency than traditional Boost PFC due to the reduction of semiconductor numbers in current flowing path. Reference [8] gives a systematic comparison of five popular Boost-cell BPFCs and a conventional Boost PFC converter. Figs. 1 and 2 from reference [8] shows the EMI and efficiency performances of six PFC topologies based on simulation. According to its conclusion, Two-Boost-Circuit BPFC in Fig. 3 shows better performances than others due to the system efficiency improvement without inducing EMI problems.

In the Two-Boost-Circuit BPFC, during the positive AC line, diode D_1 operates when MOS S_1 turns off, and Boost inductor L_1 discharges, meanwhile giving energy to load. When MOS S_1 turns on, Boost inductor is charged, and diode D_1 is off. The output capacitor discharges and transfers energy to load. Line frequency diode D_3 returns the current from output to neutral and reduces common mode (CM) noise. In the negative AC line, the PFC works symmetrically.

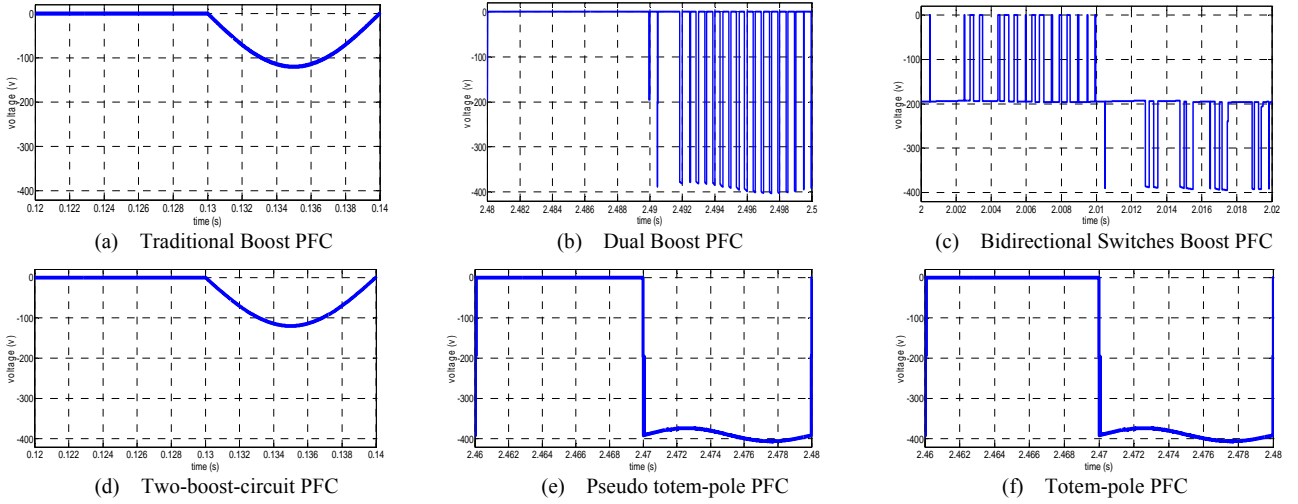


Fig. 1. CM voltage waveforms between power ground and the neutral of ac source showing the EMI comparison among the six PFC topologies [8].

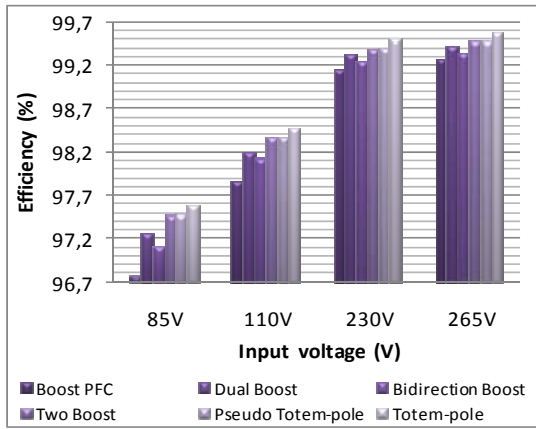


Fig. 2. Efficiency comparison only for conduction losses among six PFC topologies based on simulation [8].

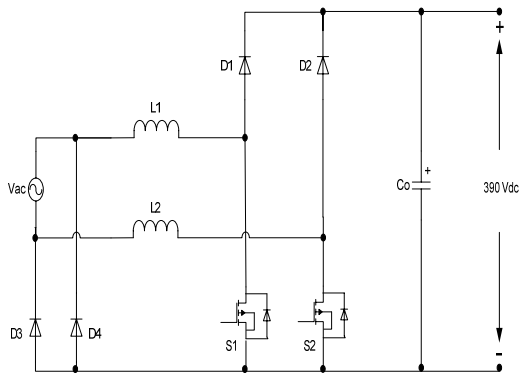


Fig. 3. Two-Boost-Circuit BPFC

If the PFC runs in continuous current mode (CCM), the average changing energy stored in the Boost inductors in each switching cycle should be approximate zero in steady states. So the input and output transfer function of BPFC in Fig. 3 is the same as a normal Boost PFC:

$$V_o = \frac{\sqrt{2} \times V_{in,rms} \times |\sin(2\pi f_s t)|}{1 - d(t)} \quad (1)$$

Where V_o is output voltage, $V_{in,rms}$ is AC rms input voltage, f_s is switching frequency and $d(t)$ is duty ratio varied with time.

III. BOOST INDUCTOR OPTIMIZATION PROCEDURE

Magnetic design is always a critical and complex part of PFC converters. A proper inductor design will not only increase the efficiency of whole system, but give a more compact and reliable PFC. However, the method for Boost PFC inductor design has been ambiguous for a long time due to the lack of effective way to evaluate the overall performances of PFC inductors. References [9] and [10] are application notes for various PFC inductors design from different well known manufacturers. In these materials, the design methods contain many experiential equations. Following these application notes will certainly lead to a quick PFC inductor design, but it is doubtful whether they have been optimized or not.

Reference [11] introduced another easy design method for PFC inductors using the “PL Product Curves”. Where, “PL” is the product of output power and Boost inductance. In this paper, the writer neglected some detailed magnetic factors which affect system performances for sure and also used many experiential results. Therefore, even this method made the inductor design easier; it is unclear if the “PL Curves” will help to get a suitable inductor design.

In order to overcome this tough problem, an optimization routine is carried out based on the high efficiency Two-Boost-Circuit BPFC in Fig. 3 operating in CCM. Its flowchart is in Fig. 4. Basically this routine can be used for any Boost type PFCs working in CCM as well.

In the optimization, considering the EMI requirement, it is a good idea to limit the switching frequency to a region from 50kHz to 70kHz to reduce the size of the EMI filter, as the filter’s size is mostly proportional to the peak amplitudes of harmonics with frequencies higher than 150kHz. Because the harmonics’ amplitudes attenuate with frequencies, it could be better to leave the maximum amplitudes of the harmonics (the first and second harmonics) with frequencies lower than 150kHz, beyond the frequency range of the EMI standard. In this way, the size of the EMI filter will be reduced with no doubt.

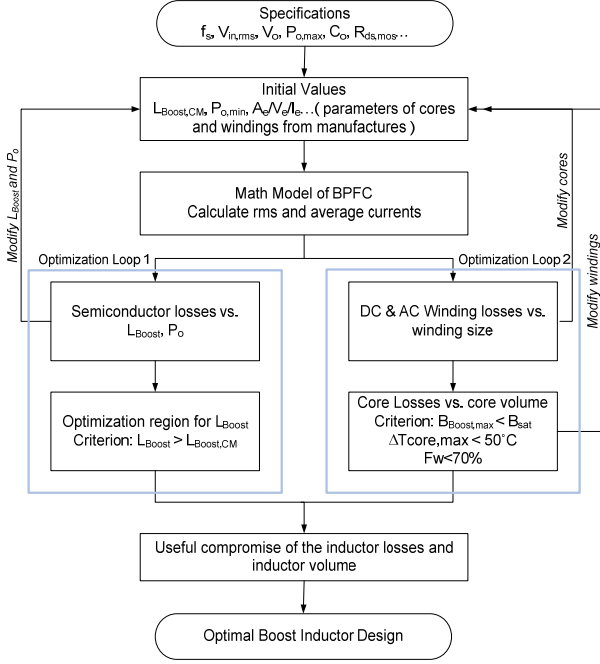


Fig. 4. Optimization procedure of inductor design in CCM for Two-Boost-Circuit BPFC with a balance of efficiency and power density.

The start point of this procedure is the specifications, which defining every fixed parameters in the main circuit. For example: input and output voltages, output peak power, output capacitors, inner parameters of the semiconductors and so on. Next, the important initial starting values of the PFC variables are set. Such as: minimal CCM Boost inductance $L_{B,CM}$, starting output power $P_{0,min}$, parameters of cores and windings from manufacturers. With all the specifications and initial values, the mathematical BPFC model will calculate the necessary rms and average currents flowing through all the components in the circuit, therefore semiconductor losses and inductor losses can be predicted.

Furthermore, inner optimization loop 1 seeks the characteristics of semiconductor losses vs. Boost inductance and output power, which will give a suitable region of Boost inductance at certain power level. And inner optimization loop 2 gets a compromise of volume and efficiency of the inductor. Both of the optimization loops will be explained in details in section IV and V. The optimal design can be realized by running optimization loop 1 and 2 together.

IV. OPTIMIZATION LOOP 1 – INDUCTANCE OPTIMIZATION

The mathematical model should be able to predict the rms and average currents of the BPFC for calculating losses. In Table I, the necessary normalized average and rms currents in one switching cycle running through the semiconductors of the BPFC in Fig. 3 are summarized under CCM and DCM conditions. Normalization process has been taken in order to make the comparison more clear. The normalization standards are given in Table II according to what were proposed in references [12] and [13]. Where the subscript “n” means normalized, T_L and T_s are line period and switching period, v and i are instant voltage and current in the PFC. Because the PFC is

working symmetrical, only the currents running in S_1 , D_1 and D_3 are discussed here. The derivations are described in details in the Appendix.

In Table I: d is the MOSFET on duty ratio; d_1 is the conduction duty ratio of the Boost diodes in DCM; $\Delta i_{L,n}$ is the inductor ripple current; the $i_{pk,n}$ is the peak inductor current in DCM; $i_{in,n}$ and $v_{in,n}$ are the normalized instant current and voltage.

From Table I and II it can be seen: the semiconductor losses are as the functions of Boost inductance.

Fig. 5 displays the semiconductor loss ratio (including conduction and switching losses) as a function of the output power and Boost inductance when the input voltage is 220Vac and output voltage is 390V. Fig. 5 shows:

1. When increasing Boost inductance, at the beginning, the semiconductor losses reduce significantly. However, as soon as the Boost inductance reaches 0.6mH, the losses reduction vs. Boost inductance is not evident any more.
2. If the PFC operates in the variable load application, there will be a suitable region for Boost inductance selection. Inside this region, the PFC system should have relatively lower semiconductor losses and higher power density.

According to Fig. 5, we can see: it is not needed to use a very large Boost inductor to reduce semiconductor losses and components' stresses in Two-Boost-Circuit BPFC. An inductance range from 0.2mH to 0.6mH should be a suitable region for 300W up to 3.2kW application, because it will achieves a good balance between semiconductor losses and inductor volume. As the inductor's volume is approximately proportional to the inductance when the stored energy is constant [14]:

$$V_L = 0.5\alpha_V L I_L^2 \quad (1)$$

Where V_L is the inductor volume, α_V is a technical factor of the inductance and relates the volume to the stored energy.

TABLE I. CURRENTS OF SEMICONDUCTORS IN ONE SWITCHING CYCLE IN CCM AND DCM CONDITIONS FOR LOSSES CALCULATIONS

	$i_{S1,rms,n}$	$i_{D1,av,n}$	$i_{D3,av,n}$
CCM	$\sqrt{d(n) \left(i_{in,n}^2(n) + \frac{\Delta i_{LB,n}^2(n)}{12} \right)}$	$(1-d(n)) \cdot i_{in,n}(n) $	$ i_{in,n}(n) $
DCM	$i_{pk,n} \cdot \sqrt{\frac{d(n)}{3}}$	$d_1(n) \cdot \frac{i_{pk,n}(n)}{2}$	$ i_{in,n}(n) $

TABLE II. NORMALIZED VOLTAGE, CURRENT AND INDUCTANCE

$v_n = \frac{v}{V_o}$	$i_n = \frac{i}{I_o}$	$L_n = L \frac{I_o}{V_o T_s}$
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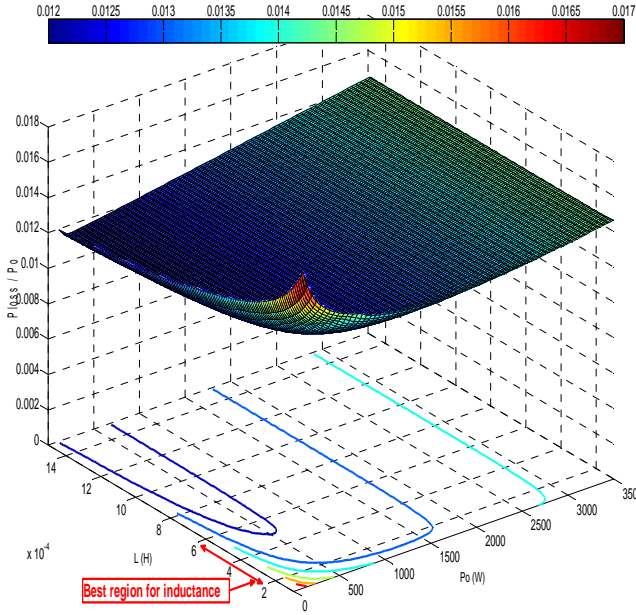


Fig. 5. Semiconductor loss ratio vs. Boost inductance and output power level

V. OPTIMIZATION LOOP 2 – INDUCTOR EFFICIENCY AND VOLUME OPTIMIZATION

Boost inductors occupies the majority of volume in PFC converters. In order to make a compact PFC converter, the inductor design should be paid high attention. Furthermore, the power losses in the inductors have a relationship with the inductors' size as well. In optimization loop 2, an optimized compromise between size and efficiency of a Boost inductor can be achieved.

A. Cores Selection

It is well known that the inductor losses come from core losses and winding losses. In order to predict the inductor losses, the first step is the core selection. A good core for Boost inductor must have high flux saturate limitation, low core losses and acceptable price. On the magnetic manufacturers' website, there will be very specific information about each core and its material, which can be used as references. In this design procedure, the Kool Mu E cores were chosen because of their advantages of high saturation level, relatively low core losses and cheaper to get. All the details of Kool Mu E cores will be defined as initial values at the beginning of the optimization procedure.

B. Winding Losses

Considering the winding losses, the DC part will keep the same in a constant power if the size and length of the winding is fixed; however the AC losses is more complex due to the skin and proximity effects. In this design, copper foil was used in order to decrease the proximity effect. Eqs. (2) - (5) give the functions of winding losses, switching frequency, layers and copper foil thickness [15]. Where, h is the thickness of copper foil, δ is skin depth, and ϕ is the ratio between copper thickness and skin depth.

$$P_w = \phi \cdot \left[G_1(\phi) + \frac{2}{3}(M^2 - 1)[G_1(\phi) - 2G_2(\phi)] \right] \times P_{dc} \quad (2)$$

$$\phi = \frac{h}{\delta} = \frac{h\sqrt{f_s}}{7.5} \quad (3)$$

$$G_1(\phi) = \frac{\sinh(2\phi) + \sin(2\phi)}{\cosh(2\phi) - \cos(2\phi)} \quad (4)$$

$$G_2(\phi) = \frac{\sinh(\phi)\cos(\phi) + \cosh(\phi)\sin(\phi)}{\cosh(2\phi) - \cos(2\phi)} \quad (5)$$

According to the equations above, Fig. 6 shows the increase of layer copper losses producing by proximity effect vs. ϕ and MMF force ratio m .

It can be seen in Fig. 6, with the factor ϕ and MMF ratio m increasing, the AC losses increase significantly. Therefore, copper foil can limit AC losses comparing to round windings due to the reduction of factor ϕ .

Since the methods for decreasing AC and DC losses are against each other - low AC losses asks for thin copper foils, but low DC losses requires thick copper foils, it is useful to find out which affects winding losses more. Assuming the switching frequency is 65kHz, and all the simulations are under the same condition: 220Vac input and 390V output at 3.2kW. Because the variation trend of inductor winding losses are independent on the cores, in Fig. 7, the inductor winding losses vs. thickness of copper foil (symbolized by h) and inductance are given for Kool Mu E core 5528E090 from Magnetics® as an example.

It can be seen that at the same inductance: on one hand, when the copper foil thicknesses increase, the total winding losses reduce due to DC losses reduction. That means in high power BPFC, DC winding losses dominate total winding losses. But on the other hand, the maximum inductance which can be wound on the core decreases as h getting thicker, that's because of the windows area limitation. However this will not worsen the semiconductor losses as long as carefully choosing the suitable inductance according to what has been mentioned in section IV.

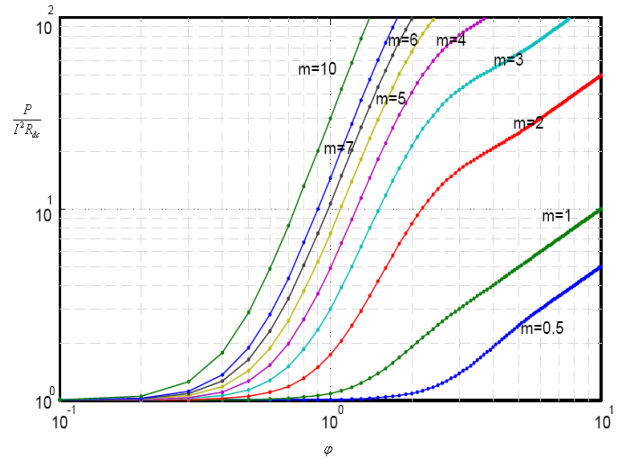


Fig. 6. Increase of layer copper losses producing by proximity effect as a factor ϕ and MMF force ratio m [14].

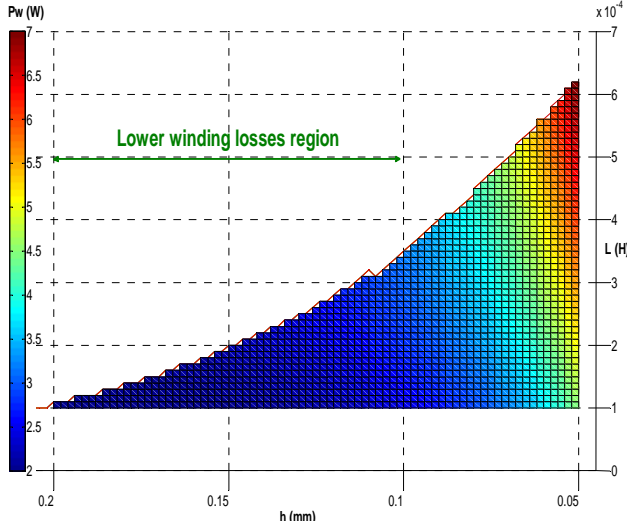


Fig. 7. Inductor winding losses vs. thickness of copper foil and inductance. The core is Kool Mu E core 5528E090 from Magnetics®.

Since the variation trend in winding losses will keep the same in different cores, considering the total amount of AC and DC losses reduction, h varies from 0.1mm to 0.2mm can be a good range for keeping lower winding losses.

C. Core losses

Eq. (6) gives the function of core losses, flux density, switching frequency and the volume of the Kool Mu cores [16].

$$P_{core} = K_H f_s^\beta B_{av}^\alpha V_e \quad (6)$$

Where K_H , α and β are constant parameters, which are determined by the material of the core. V_e is the volume of the core.

B_{av} is the average flux density in the core during half line period. It can be calculated as below:

$$B_{av} = \frac{1}{N'} \sum_{n=1}^{N'} \frac{v_L(n) \cdot d(n)}{2N A_e f_s} \quad (7)$$

Where the $v_L(n)$, $d(n)$ are the instant values of inductor voltage and switch duty ratio at each switching cycle. N is the turns of the inductor and A_e is cross section of the core. N' is the number of switching cycles in a half line cycle, which is the greatest integer of $f_s/2f_L$.

From Eqs. (6) and (7), Fig. 8 shows the core losses vs. Boost inductance for all the qualified Kool Mu E cores from Magnetics® [17]. In the legend on the top right corner, the cores were ranked by their sizes, the top the smaller.

According to Fig. 8, it is clear that when the inductance increases, the core losses decrease due to the increase of turns.

Fig. 9 shows the total Boost inductor losses vs. inductance for different qualified Kool Mu E cores from Magnetics® when h equals to 0.13mm. From Fig. 9, comes to the conclusion:

1. At a constant power, the inductor losses have its minimal value while inductance increases.

2. The minimal inductor losses are affected by the cores. However, this relationship is not exactly the same as: the bigger the core, the lower the losses. It depends on several factors. Such as geometry of core, permeability, DC bias performances and temperature rising. For example, at the same inductance, core 5528E090 (43.1cm³) is smaller than 8020E040 (72.1cm³), but its inductor losses are lower due to its higher permeability.
3. Using core 5528E090 and 0.13mm copper foil, the highest power density and relatively low inductor losses can be achieved in the same system.

Table III shows the volumes of all the qualified E cores, their minimal inductor losses and power density at 3.2kW in Fig. 8. It should be noted; cores 7228E060 and 5530E090 could be also nice choices for higher efficiency but slightly lower power density applications. However, because they were very hard to get and cost too much, we didn't select them.

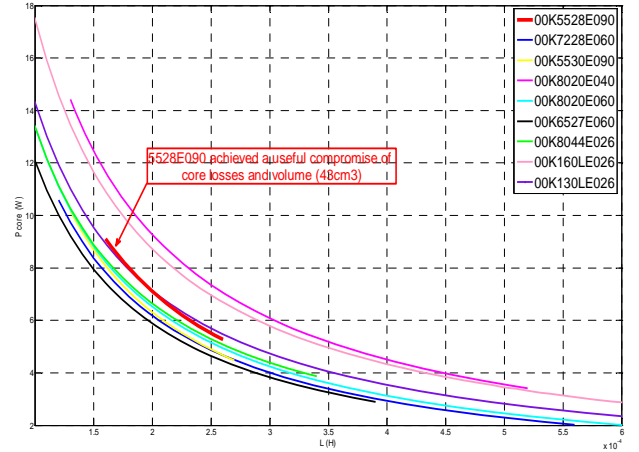


Fig. 8. Core losses vs. Boost inductance of all the qualified Kool Mu E cores from Magnetics®.

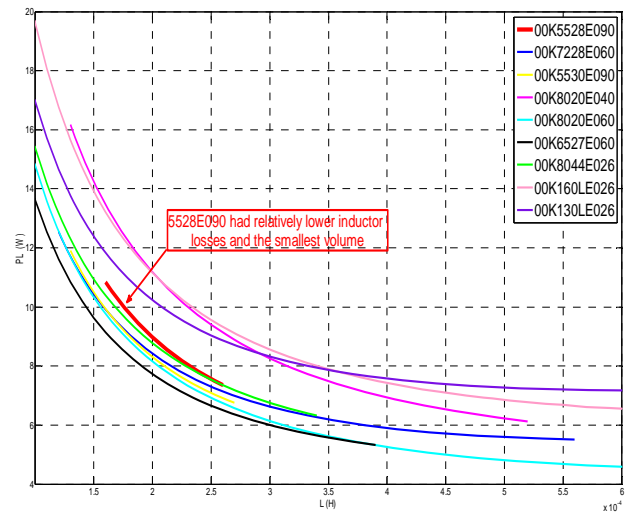


Fig. 9. Total inductor losses vs. Boost inductance for all the qualified Kool Mu E cores from Magnetics® when $h=0.13$ mm.

TABLE III. VOLUMES, LOSSES AND POWER DENSITY OF QUALIFIED KOOL MU E CORES FROM MAGNETICS®

Core Number	Volume (cm ³)	Min. P _L (W)	Power Density (W/cm ³)
00K5528E090	43.1	7.4	37.1
00K7228E060	50.3	5.5	31.8
00K5530E090	51.4	6.8	31.1
00K8020E040	72.1	6.1	22.2
00K8020E060	72.1	4.6	22.2
00K6527E060	79.4	5.3	20.2
00K8044E026	80.9	6.3	19.8
00K160LE026	212.0	6.6	7.5
00K130LE026	237.0	7.2	6.8

VI. EXPERIMENTAL VERIFICATION

According to section IV and V, the optimized Boost inductor parameters for the Two-Boost-Circuit BPFC in Fig. 3 at 3.2kW and 220Vac input can be: $L=0.23\text{mH}$, the copper foil is 0.13mm , using Kool Mu E core 5528E090 (volume is 43.1mm^3) for both high efficiency and high power density application. In experimental verification, MOSs were IPW60R045CP from Infineon®; Boost diodes were implemented with STPSC1206 SiC diode from ST®; and diodes STTH6004W from ST® were used as the return diodes. Compare the calculation data to the measurement results, the efficiency curves are given in Fig. 10 from 300W to 3.2kW. Fig. 11 gives the measured input voltage and current waveforms of this BPFC at 3.2kW.

In Fig. 10, the measured results match the calculated results very well above 1500W. However, in the low power level, the calculated efficiency is a little lower than measurement. That mainly comes from the inductor DC bias characteristics simulation. Because when the input power reduces, the Boost inductance increases due to its lower DC bias, which will cause semiconductor losses reduction. However, it is very difficult to achieve the exact DC bias curve of 5528E090, because of the insufficient core's information from manufacturer. The lower Boost inductance we predict in light load, the worse efficiency we get.

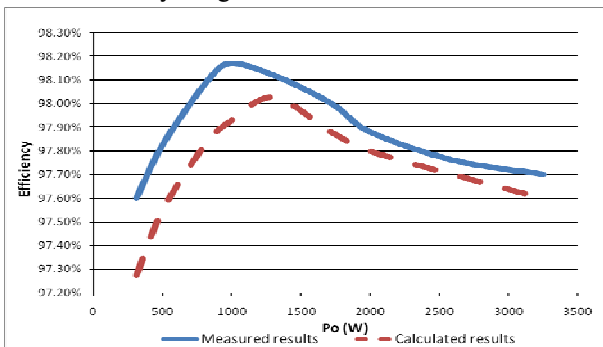


Fig. 10. Efficiency comparison of Two-Boost-Circuit BPFC at 220Vac input and 390V output using core 5528E090 from Magnetics®.

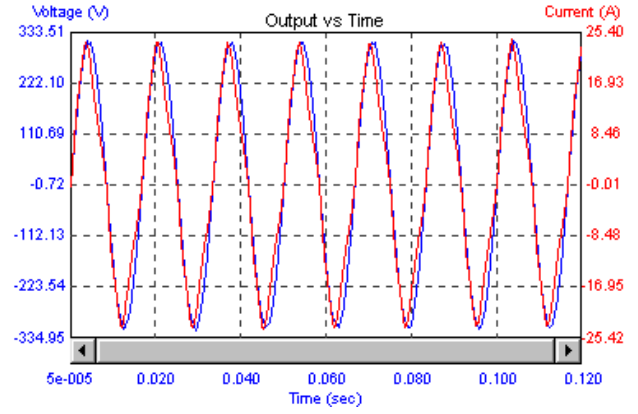


Fig. 11. Input voltage and current waveforms from Two-Boost-Circuit at 220Vac input and 390V output using core 5528E090 from Magnetics®. (PF=98.2%, Volt THD=1.1%)

It should be noted, although there were efficiency mismatches in Fig. 10, nevertheless, it can be concluded according to Fig. 10 and 11: the calculated data from the optimization design procedure will be valid to evaluate the performances of the Two-Boost-Circuit BPFC and give an optimized design between efficiency and power density of the Boost inductor.

VII. CONCLUSION

In this paper, an insight into the relationship of power, semiconductor losses, inductor losses and volumes based on a BPFC converter is given. The proposed optimization procedure is beneficial to properly compromise the efficiency and power density for Boost inductor design. Experimental verification from a 3.2kW Two-Boost-Circuit BPFC proved that the theoretical optimization procedure is applicable and can do benefits to a professional PFC design.

APPENDIX

In order to calculate system losses, the first step is to obtain the current waveform of Boost inductor. In CCM operation, its waveform during a switching cycle can be approximated as in Fig. 12. The normalized average Boost inductor current in the n th switching cycle is:

$$i_{LB,av,n}(n) = |i_{in,n}(n)| / I_o = I_{in,pk,n} \left| \sin(2\pi n \frac{T_s}{T_L}) \right| \quad (8)$$

$$n = 1, \dots, N'$$

Where T_s is the switching period, T_L is the line period.

The current ripple in Boost inductor in the n th switching cycle is determined as:

$$\Delta i_{LB,n}(n) = \frac{|v_{in}(n)|}{I_o L_{B,n}} \cdot d(n) \cdot T_s \quad (9)$$

$$= \frac{|v_{in,n}(n)|(1 - |v_{in,n}(n)|)}{L_{B,n}}$$

Where, d is the MOSFET on duty ratio. In CCM, the discrete time function is:

$$d(n) = 1 - \frac{v_{in}(n)}{V_o} = 1 - v_{in,n}(n) \quad (10)$$

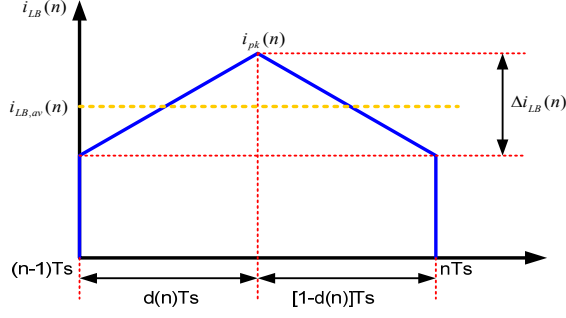


Fig. 12. Current waveform of Boost inductor in a switching cycle in CCM.

And,

$$L_B = L_{B0} \cdot \frac{A_{L,effi}}{A_{L,0}}, A_{L,effi} = f(Ni_{in}) \quad (11)$$

is the Boost inductance in different power. It is as a function of turns and input current due to the DC bias performance, which can be found in the data sheet of the cores [17].

The relevant rms and average currents for semiconductor losses calculation in CCM in the n th switching cycle are listed below:

$$i_{LB,rms,n}(n) = \frac{|i_{in}(n)|}{I_o} \cdot \sqrt{1 + \frac{1}{3} \left(\frac{\Delta i_{LB}(n)}{2i_{in}(n)} \right)^2} \quad (12)$$

$$\begin{aligned} &= \sqrt{i_{in,n}^2(n) + \frac{\Delta i_{LB,n}^2(n)}{12}} \\ i_{S1,rms,n}(n) &= \frac{|i_{in}(n)|}{I_o} \cdot \sqrt{1 + \frac{1}{3} \left(\frac{\Delta i_{LB}(n)}{2i_{in}(n)} \right)^2} \cdot \sqrt{d(n)} \\ &= \sqrt{d(n) \left(i_{in,n}^2(n) + \frac{\Delta i_{LB,n}^2(n)}{12} \right)} \end{aligned} \quad (13)$$

$$i_{D1,av,n} = (1-d(n)) \cdot \frac{|i_{in}(n)|}{I_o} = (1-d(n)) \cdot |i_{in,n}(n)| \quad (14)$$

$$i_{D3,av,n} = \frac{|i_{in}(n)|}{I_o} = |i_{in,n}(n)| \quad (15)$$

The same as the previous procedure, in DCM operation, its waveform during a switching cycle can be approximated as in Fig. 13. The normalized average current of Boost inductor in the n th switching cycle is the same as Eq. (8).

The MOSFET on duty ratio becomes:

$$d(n) = \sqrt{\frac{2(1-v_{in,n}(n)) \cdot i_{in,n}(n)}{v_{in,n}(n)}} \cdot L_{B,n} \quad (16)$$

And d_1 is the conduction duty ratio of the Boost diodes:

$$d_1(n) = \sqrt{\frac{2v_{in,n}(n) \cdot i_{in,n}(n)}{1-v_{in,n}(n)}} \cdot L_{B,n} \quad (17)$$

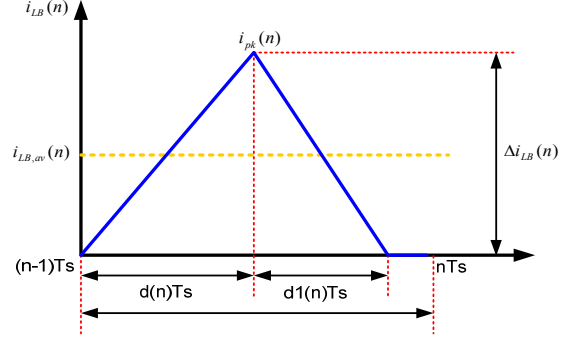


Fig. 13. Current waveform of Boost inductor in a switching cycle in DCM.

The $i_{pk,n}$ is the peak inductor current in DCM:

$$i_{pk,n}(n) = \sqrt{|i_{in,n}(n)| \cdot \frac{2|v_{in,n}(n)|(1-|v_{in,n}(n)|)}{L_{B,n}}} \quad (18)$$

The relevant rms and average currents for semiconductor losses calculation in DCM in the n th switching cycle are listed below:

$$i_{LB,rms,n}(n) = \sqrt{\frac{d(n) + d_1(n)}{3}} \cdot i_{pk,n}(n) \quad (19)$$

$$i_{S1,rms,n}(n) = i_{pk,n} \cdot \sqrt{\frac{d(n)}{3}} \quad (20)$$

$$i_{D1,av,n} = d_1(n) \cdot \frac{i_{pk,n}(n)}{2} \quad (21)$$

$$i_{D3,av,n} = \frac{|i_{in}(n)|}{I_o} = |i_{in,n}(n)| \quad (22)$$

For both CCM and DCM, the rms current flow through output capacitor is:

$$i_{Co,rms,n} = \frac{\sqrt{i_{LB,rms}^2(n) - i_{S1,rms}^2(n) - I_o^2}}{I_o} \quad (23)$$

And the corresponding normalized rms and average currents during a half line cycle are as below:

$$I_{X,rms,n} = \sqrt{\frac{1}{N'} \cdot \sum_{n=1}^{N'} i_{X,rms,n}^2(n)} \quad (24)$$

$$I_{Y,av,n} = \frac{1}{N'} \cdot \sum_{n=1}^{N'} i_{Y,av,n}(n) \quad (25)$$

Where, X symbolizes MOSs, Boost inductors and output capacitor, and Y represents Boost diodes and return diodes.

It should be noted that, since SiC Boost Diodes were used in our application, due to its excellent turn on and turn off characteristics, the switching losses can be ignored. Furthermore, even in the CCM condition, around the zero crossing of the line voltage, during a few switching cycles, the PFC operates in DCM inevitably, which was also taken into consideration during calculation in order to obtain a more precise prediction.

The CCM and DCM boundary condition happens when:

$$i_{in,n}(n) = 0.5\Delta i_{pk,n}(n) \quad (26)$$

Therefore, the time difference from the zero crossing of line voltage to DCM and CCM borderline position is also a function of inductance.

Besides, effects from temperature and current increasing which could change semiconductor and output capacitor losses were taken into consideration as well. The necessary functions can be found in the data sheet of each component [18] - [20].

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